Claims

1. (Currently Amended) A method for simulating operation of a phase lock loop circuit in an apparatus that receives external clock and external data signals for recovering a recovered clock from said external clock signal by use of said phase lock loop circuit, comprising the steps of:

digitizing said external clock signal to obtain time domain data and storing said time domain data in a memory;

detecting time domain data of edges of said external clock signal;

converting said detected time domain data of said edges of said external clock into frequency domain data;

filtering said frequency domain data by multiplying said frequency domain data by respective predetermined coefficients in different frequency domains; and

restoring the resultant frequency domain data to time domain data to obtain time domain data of edges of said recovered clock.

2. (Original) The method as recited in claim 1 wherein the coefficients are selected to simulate a filter corresponding to said phase lock loop circuit.

3. (Currently Amended) A method for measuring jitter of an external clock signal relative to a recovered clock signal in an apparatus that receives said external clock and an external data signal, said apparatus recovering said recovered clock signal from said external clock by simulating use of a phase lock loop circuit, comprising the steps of:

digitizing said external clock signal to store time domain data of said external clock in a memory;

detecting time domain data of edges of said stored external clock;

converting said detected time domain data of said edges of said external clock into frequency domain data;

filtering said frequency domain data by multiplying said frequency domain data by respective predetermined coefficients in different frequency domains;

restoring said resultant frequency domain data to time domain data to obtain time domain data of the edges of said recovered clock signal;

comparing said time domain data of the edges of said recovered clock signal with said time domain data of said stored external clock signal; and

measuring jitter of said external clock signal relative to said recovered clock signal.

4. (Original) The method as recited in claim 3 wherein said coefficients are selected to simulate a filter corresponding to said phase lock loop circuit.

5. (Currently Amended) A method for measuring jitter of an external data signal relative to a recovered clock signal in an apparatus that receives an external clock and said external data, and recovers said recovered clock from said external clock by simulating a phase lock loop circuit, comprising the steps of:

digitizing said external clock signal and said external data signal and storing resulting the time domain data of said external clock and said external data signals in a memory;

detecting time domain data of edges of said stored external clock;

converting said detected time domain data of said edges of said external clock into frequency domain data;

filtering said frequency domain data by multiplying said frequency domain data by respective predetermined coefficients in different frequency domains;

restoring resultant frequency domain data to time domain data to obtain time domain data of edges of said recovered clock;

comparing said obtained time domain data of said edges of said recovered clock with said time domain data of said stored external data; and

measuring jitter of said external data signal relative to said recovered clock.signal

6. (Original) The method as recited in claim 5 wherein said coefficients are selected to simulate a filter corresponding to said phase lock loop circuit.

7. (Currently Amended) An apparatus for simulating a recovered clock signal for use in an apparatus that receives external clock and external data signals, said apparatus recovering said recovered clock signal from said external clock signal by use of a phase lock loop, comprising:

means for digitizing said external clock to store resulting time domain data in a memory;

means for detecting time domain data of edges of said external clock signal;

means for converting said detected time domain data of said edges of said external clock signal into frequency domain data;

means for filtering said frequency domain data by multiplying said frequency domain data by respective predetermined coefficients in different frequency domains; and

means for restoring resultant frequency domain data to time domain data to obtain time domain data of edges of said recovered clock signal.

8. (Original) The apparatus as recited in claim 7 further comprising:

means for comparing said time domain data of said edges of said recovered clock signal with time domain data of said stored external clock signal; and

means for measuring jitter of said external clock signal relative to said recovered clock signal.

9. (Original) The apparatus as recited in claim 7 further comprising:

means for digitizing said external data to store resulting the time domain data in a memory;

means for comparing said obtained time domain data of said edges of said recovered clock signal with said time domain data of said stored external data signal; and

measuring jitter of said external data signal relative to said recovered clock signal.

10. (Original) The apparatus as recited in claim 7, 8, or 9 wherein said coefficients are selected to simulate a filter corresponding to said phase lock loop.